What is claimed is:

[Claim 1] A field effect transistor ("FET"), comprising:

a gate stack overlying a single-crystal semiconductor region of a substrate, said single-crystal semiconductor region having a first composition

a pair of first spacers disposed over opposite sidewalls of said gate stack;

a pair of regions consisting essentially of a single-crystal semiconductor alloy having a second composition different from said first composition, said semiconductor alloy regions disposed on opposite sides of said gate stack, each said semiconductor alloy region spaced a first distance from said gate stack; and

a pair of a source region and a drain region at least partly disposed in respective ones of said semiconductor alloy regions, said source region and said drain region each spaced a second distance from said gate stack by a first spacer of said pair of first spacers, said second distance being different from the first distance.

[Claim 2] The FET as claimed in claim 1, wherein said second distance is longer than said first distance.

[Claim 3] The FET as claimed in claim 2, wherein said single-crystal semiconductor region consists essentially of silicon and said semiconductor alloy regions consist essentially of silicon germanium.

[Claim 4] The FET as claimed in claim 3, wherein said silicon germanium regions are at least partly disposed in trenches disposed in said single-crystal silicon region.

[Claim 5] The FET as claimed in claim 4, wherein said substrate is a silicon-on-insulator (SOI) substrate and said single-crystal silicon region is disposed above a buried oxide layer of said SOI substrate.

[Claim 6] The FET as claimed in claim 5, wherein said silicon germanium regions have bottom edges disposed at a depth of about 80% or greater of a depth of a top of said buried oxide layer from a top surface of said single-crystal silicon region.

[Claim 7] The FET as claimed in claim 6, wherein the depth of said bottom edges is about 90% of the depth of said top of said buried oxide layer.

[Claim 8] The FET as claimed in claim 7, further comprising extension regions underlying said first spacers and at least partly underlying said gate stack.

[Claim 9] The FET as claimed in claim 8, further comprising halo regions underlying sad first spacers and at least partly underlying said gate stack.

[Claim 10] The FET as claimed in claim 8, wherein said sidewalls of said gate stack are oxidized, wherein said first spacers are disposed over said oxidized sidewalls.

[Claim 11] The FET as claimed in claim 10, further comprising forming second spacers disposed laterally outward from said first spacers.

[Claim 12] The FET as claimed in claim 11, further comprising silicide regions overlying said silicon germanium regions, said silicide regions spaced from said gate stack by said first spacers and said second spacers.

[Claim 13] The FET as claimed in claim 12, wherein said gate stack includes a gate silicide region and a polycrystalline semiconductor region, said gate silicide region overlying and self-aligned to said polycrystalline semiconductor region.

[Claim 14] A field effect transistor ("FET"), comprising:

a gate stack overlying a single-crystal silicon region of a silicon-on-insulator substrate;
a pair of first spacers disposed over opposite sidewalls of said gate stack;
a pair of regions consisting essentially of single-crystal silicon germanium disposed on opposite sides of said gate stack, each said silicon germanium region spaced a first distance from said gate stack;
a pair of a source region and a drain region at least partly disposed in respective ones of said silicon germanium regions, said source region and said drain region each spaced a second distance from said gate stack by a first spacer of said pair of spacers; and
silicide regions, at least one of said silicide regions disposed as a layer of said gate stack, and at least one of said silicide regions at least partly overlying said silicon germanium regions.

[Claim 15] A method of fabricating a field effect transistor ("FET"), comprising:

patterning a gate polycrystalline semiconductor layer overlying a single crystal semiconductor region of a substrate having a first composition to form a gate polyconductor ("PC");
forming sacrificial spacers overlying sidewalls of said PC;
recessing portions of said single crystal semiconductor region in locations adjacent to said sacrificial spacers;
epitaxially growing regions consisting essentially of a single crystal semiconductor alloy in said locations, said semiconductor alloy regions having

a second composition different from said first composition, such that said sacrificial spacers at least partly determine first spacings between said semiconductor alloy regions and said PC;
removing said sacrificial spacers; and
completing said FET.

[Claim 16] The method as claimed in claim 15, wherein said single-crystal semiconductor region consists essentially of silicon and said semiconductor alloy regions consist essentially of silicon germanium.

[Claim 17] The method as claimed in claim 16, wherein said step of completing said FET includes forming second spacers overlying sidewalls of said PC and performing source and drain implants to at least said silicon germanium regions, using said PC and said second spacers as a mask.

[Claim 18] The method as claimed in claim 17, wherein locations of source and drain regions of said FET are determined by said source and drain implants, and said second spacers at least partly determine second spacings between said source and drain regions and said PC.

[Claim 19] The method as claimed in claim 18, wherein said first spacings are different from said second spacings.

[Claim 20] The method as claimed in claim 19, wherein said step of completing said FET further includes performing at least one of an extension implant and a halo implant prior to forming said second spacers.

[Claim 21] The method as claimed in claim 16, wherein said silicon region is disposed in a silicon-on-insulator (SOI) layer of said substrate overlying a buried oxide layer of said substrate.

[Claim 22] The method as claimed in claim 21, wherein said step of recessing said portions of said silicon region includes implanting said portions and preferentially etching said implanted portions relative to portions of said silicon region which are not implanted by said implanting.

[Claim 23] The method as claimed in claim 22, wherein a depth of said implanting determines a recess depth to which said portions are recessed.

[Claim 24] The method as claimed in claim 23, wherein said recess depth extends to about 80% or greater to a depth of a top of said buried oxide layer from a top surface of said silicon region.

[Claim 25] The method as claimed in claim 24, wherein said recess depth extends to about 90% of said depth of said top of said buried oxide layer.

[Claim 26] The method as claimed in claim 23, wherein said implanting implants germanium into said silicon regions.

[Claim 27] The method as claimed in claim 26, further comprising forming third spacers over said second spacers, and forming a silicide overlying said silicon germanium regions, said silicide spaced from said PC by said second spacers and said third spacers.

[Claim 28] The method as claimed in claim 27, further comprising oxidizing said sidewalls of said PC prior to forming said second spacers.

[Claim 29] The method as claimed in claim 28, wherein said sacrificial spacers include nitride spacers disposed on said oxidized sidewalls of said PC, and oxide spacers disposed on sidewalls of said nitride spacers.

[Claim 30] The method as claimed in claim 29, further comprising forming a gate silicide from said polycrystalline semiconductor while simultaneously forming said silicide overlying said silicon germanium regions.